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Abstract:III-V nanowire (NW) transistors are an emerging technology with the prospect of high performance and low power dissipation. Performance evaluations of these devices, however, have focused mostly on the intrinsic properties of the NW, excluding any parasitic elements. In this paper, a III-V NW transistor architecture is investigated, based on a NW array with a realistic footprint. Based on scaling rules for the structural parameters, 3-D representations of the transistor are generated, and the parasitic capacitances are calculated. A complete optimization of the structure is performed based on the RF performance metrics f<inf>T</inf> and f<inf>max</inf>, employing intrinsic transistor data combined with calculated parasitic capacitances and resistances. The result is a roadmap of optimized transistor structures for a set of technology nodes, with gate lengths down to the 10-nm-length scale. For each technology node, the performance is predicted, promising operation in the terahertz regime. The resulting roadmap has implications as a reference both for benchmarking and for device fabrication. © 2012 IEEE.
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