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Title:Thermal performance of CMOS-SOI transistors from weak to strong inversion
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Abstract:A promising solution to continue the complementary metal-oxide semiconductor (CMOS) scaling roadmap at the 22 nm technology node and beyond is CMOS-silicon on insulator (SOI), which is used especially in low-power and "system on chip" applications. CMOS-SOI involves building conventional MOSFETs on very thin layers of crystalline silicon. The thin layer of silicon is separated from the substrate by a thick layer of buried SiO₂ film, thus isolating the devices from the underlying silicon substrate and from each other. CMOS-SOI technology is already a leading technology in a wide range of applications where integrated CMOS-SOI-microelectromechanical systems or nanoelectromechanical systems (MEMS/NEMS) technologies provide unique sensing systems for IR and terahertz (THz) imagers. CMOS-SOI technology is traditionally classified into partially depleted (when the silicon device layer is thicker than the maximum gate depletion width) and fully depleted devices (when the device layer is fully depleted before the threshold voltage is reached). It may also be classified, like all CMOS technology, according to the minimal channel length, L_{min}. This study focuses on partially depleted 0.18 RF CMOS-SOI technologies [4] with emphasis on the weak and strong inversion regions. This process is suitable for mixed-signal design because of its maturity and relatively low cost, while the methodology and results presented here may be extended to any advanced CMOS-SOI nano-transistors. The results of this study may provide a systematic approach to assessing the thermal behavior of CMOS-SOI transistors operating in a wide range of temperatures.
Number of references:10
Inspec controlled terms:CMOS integrated circuits - low-power electronics - MOSFET - nanoelectronics - semiconductor thin films - silicon compounds - silicon-on-insulator - thermal analysis
Uncontrolled terms:thermal performance - CMOS-SOI transistor technology - complementary

metal-oxide semiconductor scaling roadmap - CMOS-silicon-on-insulator - system-on-chip - MOSFET - crystalline silicon - integrated CMOS-SOI-microelectromechanical systems - nanoelectromechanical systems - MEMS-NEMS technology - terahertz imagers - IR imagers - fully depleted devices - mixed-signal design - CMOS-SOI nanotransistors - size 22 nm - SiO_2 - Si

Inspec classification codes:B2560R Insulated gate field effect transistors - B2570D CMOS integrated circuits

Numerical data indexing:size 2.2E-08 m

Chemical indexing:SiO2/int O2/int Si/int O/int SiO2/bin O2/bin Si/bin O/bin;Si/sur Si/el

Treatment:Practical (PRA)

Discipline:Electrical/Electronic engineering (B)

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